State-of-the-Art CMOS Image Sensors: Looking Under the Hood

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Pixel development over the last five decades has been on a trajectory that adds process complexity to achieve the performance required for imaging. A hero in this effort has been the process engineers, both development and manufacturing, who have managed a series of image-sensor-specific enabling process enhancements that meet the requirements for performance, yield and cost. These include process enhancements, including using new materials to reduce cross-talk, enhance optical performance, and allow added functionality (Figure 1). These can be processes carried over from other products such as MIMcaps (Figure 2) or they can be novel structures to image sensors like airgap backside grid (Figure 3).

Product development progresses as a series of technical challenges until marketing requirements are met (e.g., shrinking the pixel size to reduce cost and increase array size) and then a shift to the next marketing need (e.g., adding functionality such as high dynamic range). The purpose of reverse engineering is to document the technology development practiced by each manufacturer and anticipate upcoming decision points in the process development.

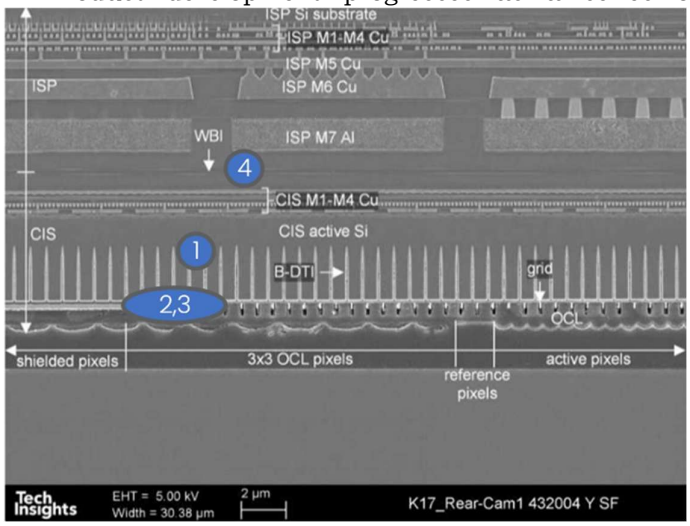


Figure 1 SK hynix Hi-5021Q: (1) photodiode; (2) backside dielectric layers; (3) backside optic structures; wafer bond & interconnect

An example of an enabling technology is stacking. The trajectory was from front-side illuminated single metal CCD's to multi-metal CMOS to add functionality to backside illuminated to improve optical response to face-to-face stacked CMOS to add image processing while limiting die size. The last required metal interconnects, initially through silicon vias located in the periphery of the die, but this is being replaced by hybrid bonding enabled by the material property that two polished SiO surfaces, when brought into contact, will form crosslinks for strength and that two polished Cu surfaces will do the same providing electrical interconnections. In practice, the SiO surfaces can just be the bulk interconnect dielectric layer. Still, other foundries find it useful to form a layer incorporating C or N and then create a thin SiO layer for bonding by a plasma treatment (Figure 4).

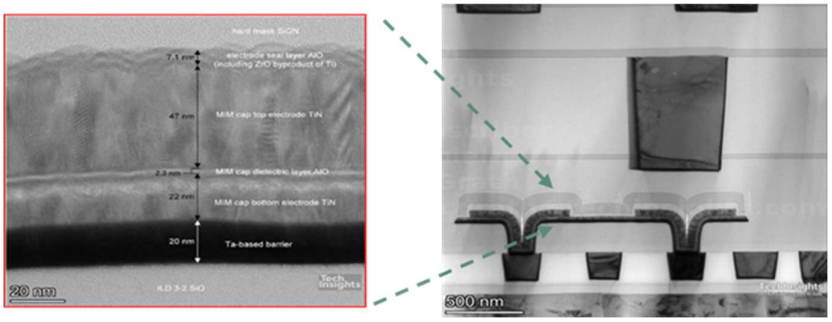


Figure 2. MIMcap: ams OSRAM Mira220 with 2.3 nm AlO/ZrO dielectric

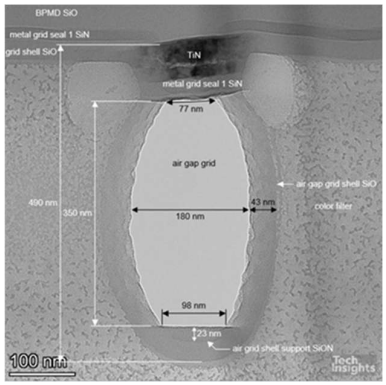


Figure 3. SK hynix Hi-5022Q backside airgap grid

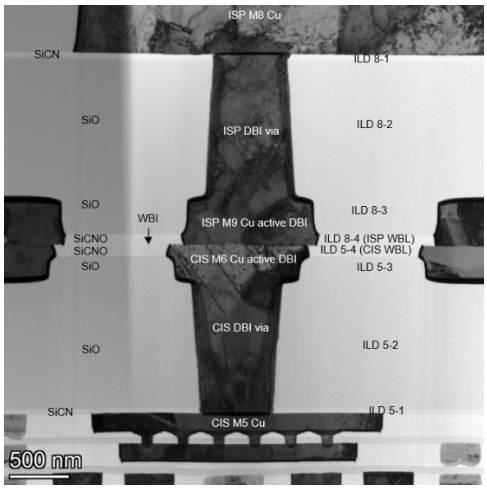
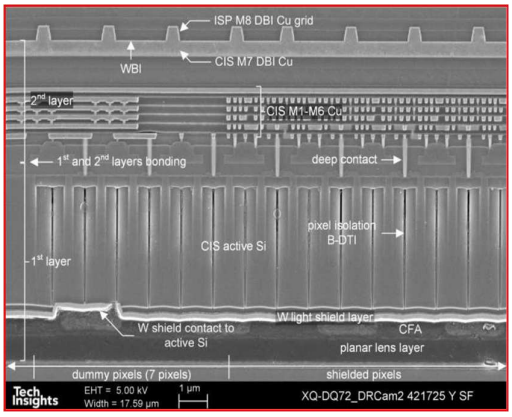


Figure 4. Samsung GM5 Cu-to-Cu interconnect

The next logical direction for image sensor stacking with pixel-wise interconnects is to go to three layers. This can mean dividing the pixel layer to optimize the photodiode free from constraints related to CMOS or separating the image signal processing layer to provide a pixel-wise signal processing array layer or adding a memory layer. The existence of a middle layer means developing a back-to-front wafer-to-wafer interconnect, whether a through silicon via with deep contact formation from one side (Figure 5) or one that provides a backside copper pad for hybrid bonding[1].

The trend for wafer-wafer interconnects pitch was technology-limited and decreased steadily until 2020. Since then, the pitch has stabilized by foundries, with each foundry having its own sweet spot. TSMC seems the most aggressive at 1.4µm.



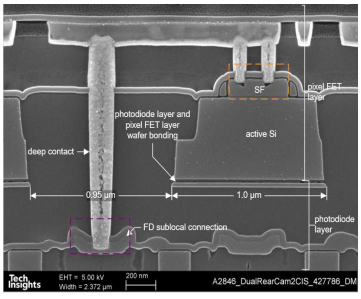


Figure 5. Sony IMX904: [L] 2-layer pixel stack; [R] pixel layers' TSVs

The sweet spot for image sensors for smartphones appears to be 50 Mpixel with pixel pitches of 0.5µm to 0.7µm. There is technical differentiation with the choice of planar or vertical transfer gates and with the implementation of dual or triple high dynamic range (Figure 6).

A feature of the smartphone pixels is the use of dual gate oxide in the pixel, thinner for the source follower and thicker for the control FETs (Figure 7).

Given that the image sensor is both an integrated circuit and a transducer, there is a need for novel structures and novel choice of materials to provide the photo-optical performance. This includes forming a backside structure to both reduce dark signal generation and enhance optical response. While there seems to be a consensus on using AlO/ZrO as the layer deposited on the backside silicon to suppress charge generation, the next layer varies between TaO and HfO by the manufacturer (Figure 8).

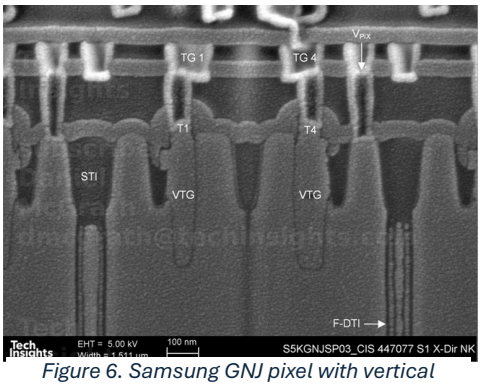
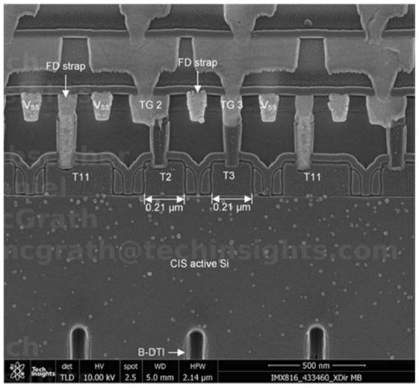
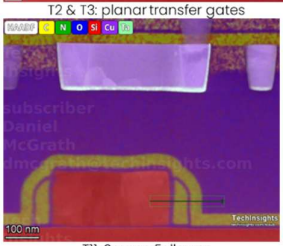


Figure 6. Samsung GNJ pixel with vertical transfer gate

A unique feature of the photodiode is the deep trench isolation, which reduces optical and prevents photocarrier crosstalk between pixels. This photodiode features an etch with an aspect ratio between 10:1 and 40:1, filled with thin conformal material layers from 10nm to >100nm (Figure 9). The materials used can include SiO, polysilicon, W, AlO, TaO and TiN.





T11: Source Follower

Figure 7. SONY IMX816 with thin gate oxide source follower

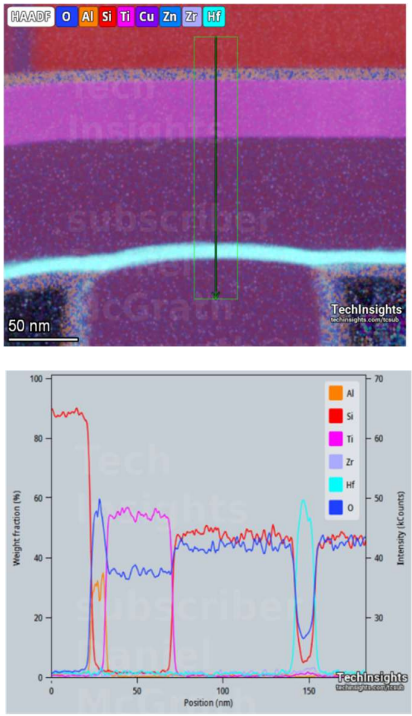


Figure 8. Samsung GNJ backside layers at grid structure

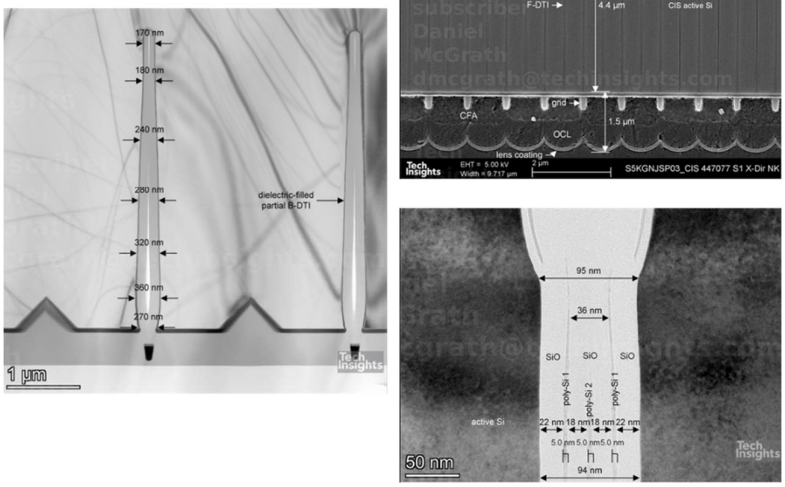


Figure 9. Deep trench isolation: [L] ams OSRAM Mira220; [R] Samsung GNJ

The momentum in pixel development has shifted from shrinking a 4T pixel or the shared version of the same to adding more functionality to the pixel. Improved capacitors are key in adding high dynamic range and global shutter. Available capacitors can be MOS capacitors, parasitic FET capacitors, interdigitated capacitors and capacitors by linking elements from adj adjacent rows. MIMcaps with the incorporation of nanometer dielectric and their placement in the interconnect layers is an enabler of small pixels with voltage domain global (Figure 2). Because of space constraints, pixels will mix single instances of capacitor types, but SmartSens has incorporated a stacked MIMcap as an alternative (Figure 10L). STMicro has incorporated pixels where capacitors are formed in the photodiode layer, either external to the deep trench isolation or inside (Figure 10R).

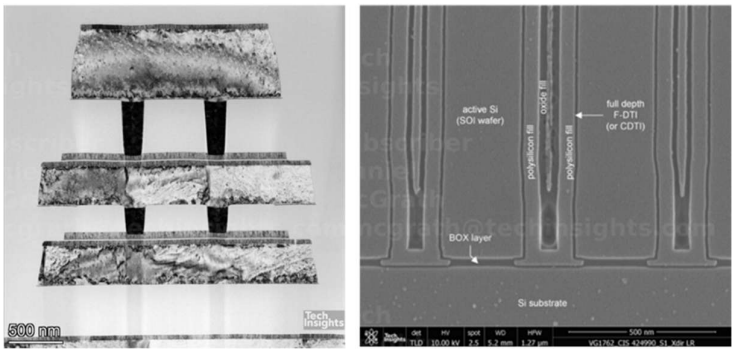


Figure 10. [L] SmartSens SC53HGS dual MIMcaps; [R] STMicro capacitors in a photodiode deep trench

The emergence of wafer-to-wafer interconnects with small pixel pitch enables SPAD sensors with 100% fill factor since the pixel circuitry can now be placed behind the photodiode (Figure 11).

Innovation or revisiting of ideas from the past is still evident in the high-end MILC camera applications. This is demonstrated by Sony incorporating a backside light pipe with an inner lens (Figure 12).

Enhanced image-sensor-specific processes have enabled non-photographic imaging opportunities. Eye tracking in an augmented reality headset requires imaging outside the visible viewing spectrum so the image sensor uses all of the tricks for the NIR: 6.4µm photodiode silicon; deep trench isolation; backside inverted pyramid arrays (Figure

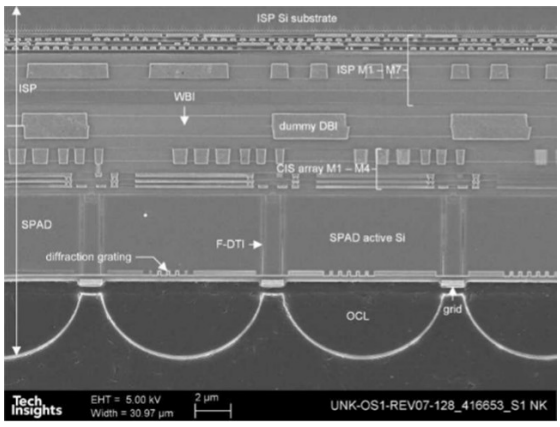


Figure 11. Ouster L3 Stacked SPAD

13). The part benefits from the small form factor provided by stacking.

The first multispectral smartphone camera uses a 3x3 color filter array with one color pixel in each created without a color filter or a microlens (Figure 14). The application appears to be for visible wavelengths to provide color correction information.

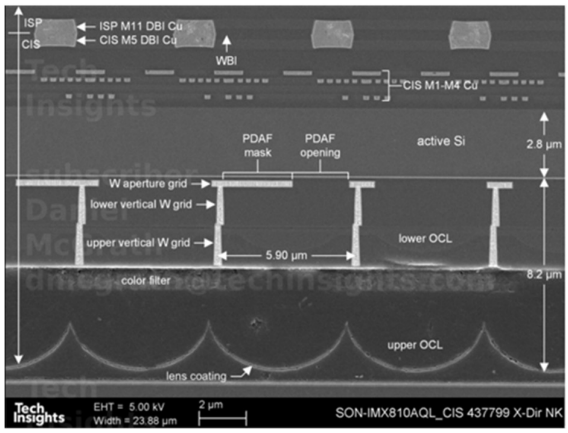


Figure 12. Sony IMX810 with backside inner lens

Imaging in the short-wave infrared (SWIR) band requires innovation for commercial applications because Si does not absorb in these wavelengths beyond 1.0µm. The challenges are manufacturability and environmental concerns related to toxic materials involved. An innovative approach that addresses the former is building a n-p junction of transparent fullerene and absorbing PbS quantum dots on top of a Si readout integrated circuit (Figure 15).

The fact that image sensor products benefit from process enhancements even as pixel sizes for applications seem stable points to the value of continued technology development. Stacking with pixel-wise interconnects is enabling the multilayer stack is an opportunity, and the shift from driving pixels smaller to making pixels with added functionality opens possibilities. We are at a point in image sensor technology where the cost-per-pixel is amazingly inexpensive, so we in the community are no longer bound to just one lead product but have a wide horizon ahead.

Reference:

(1) Gwi-Deok Ryan Lee, et al., "A 0.5µm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-pixel Cu-Cu", IEDM (2023)

Note: all images can be found in reports at TechInsights.com (https://library.techinsights.com/reverse-engineering/image-sensor-content-navigator)

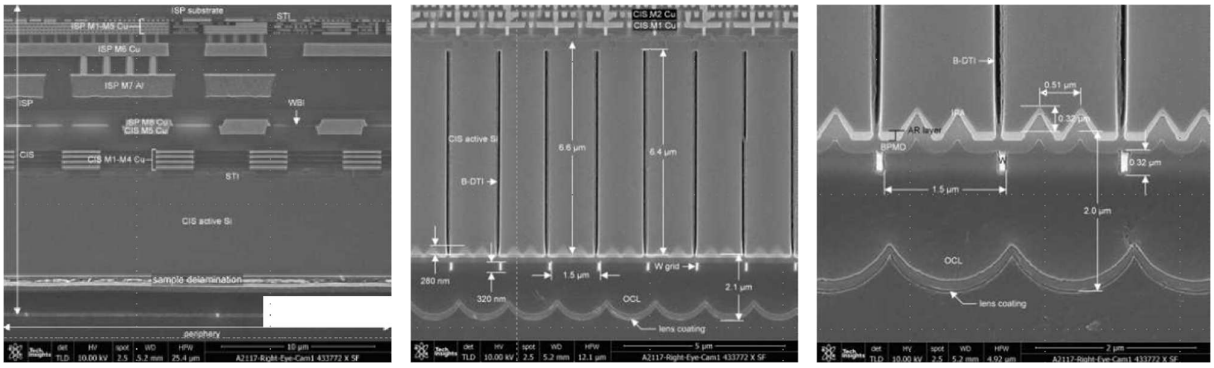


Figure 13. Apple Vison Pro Eye Tracker

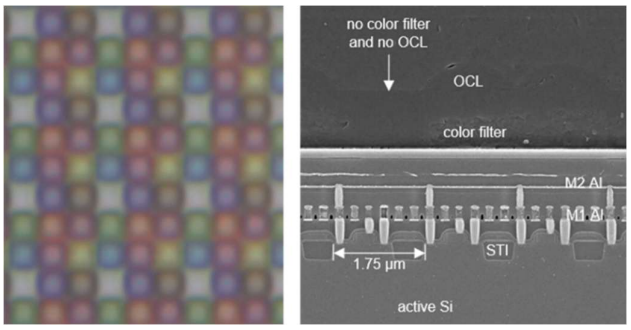


Figure 14. GalaxyCore Multispectral Image Sensor in Huawei Mate70 Pro+

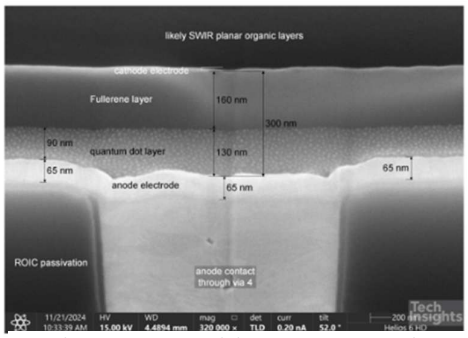


Figure 15. SWIR Vision Acuros CQD with Fullerene/PbS QD junction